Servicing Data

# OHIO SCIENTIFIC

for

## COMPUTER BOARDS 470 (Floppy), 505 Rev. A, 510 Rev. C, 520 Rev. B, 520 Rev. C, 525, 527, 535, 550, 555, 590, 592, 594

as used in

## Challenger II and III Series

Models
C2-OEM
C3-OEM
C3-A
C3-B
C3-C
C3-S1

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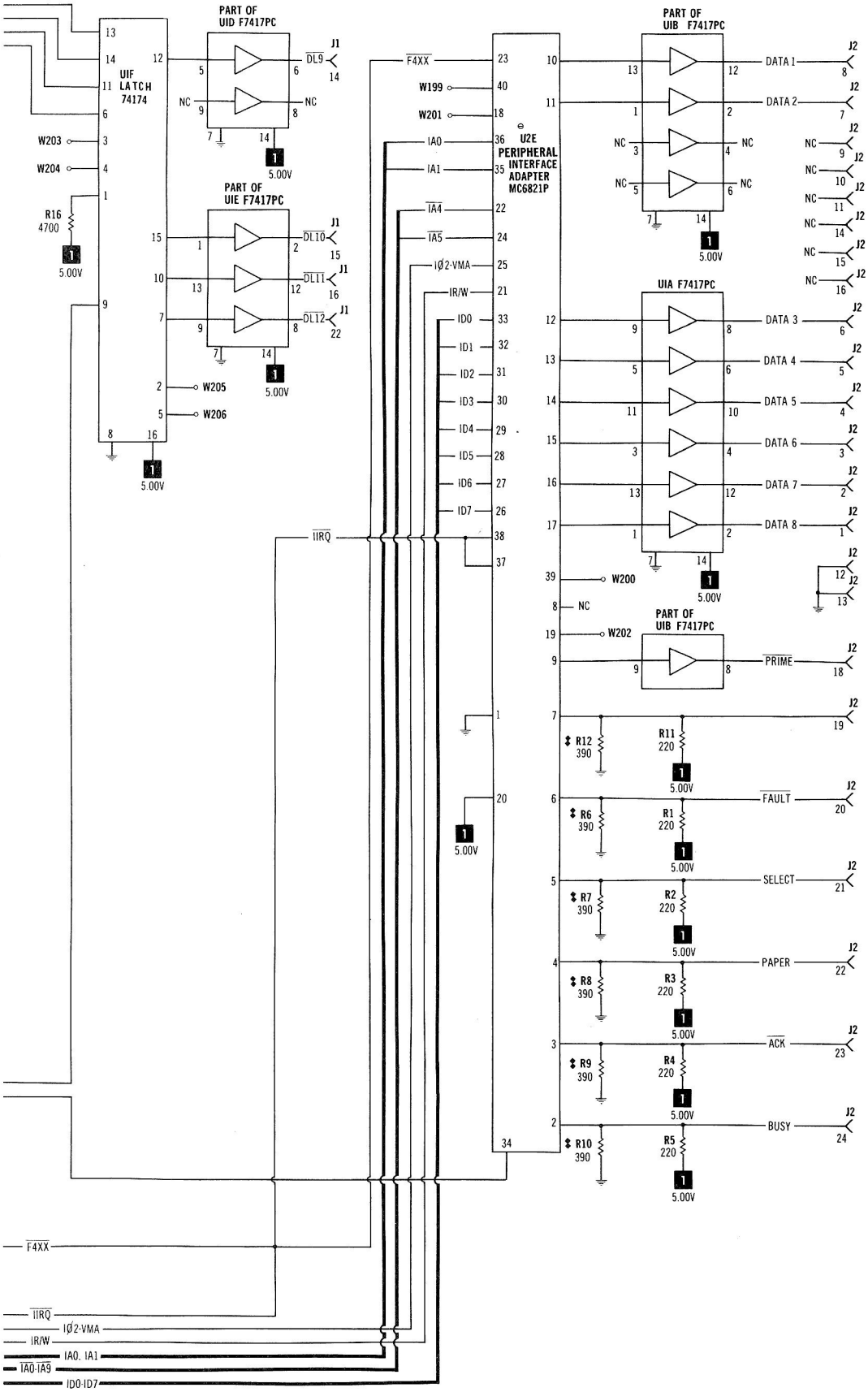
*Bunch of pages missing from here to Page 147*



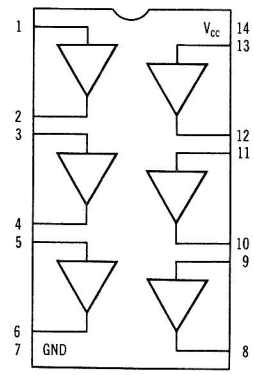



FOR SCHEMATIC LEGEND AND NOTES
SEE PAGES 180,181 & REAR COVER.

555 BOARD

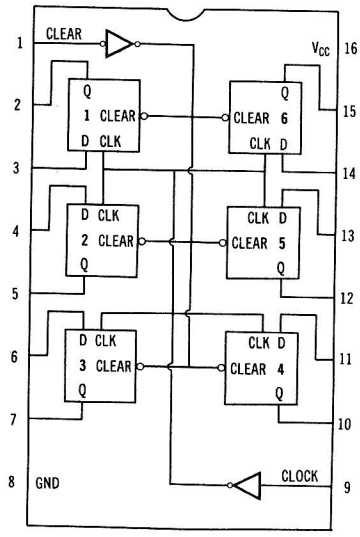
# 555 BOARD PINOUTS

F7417PC



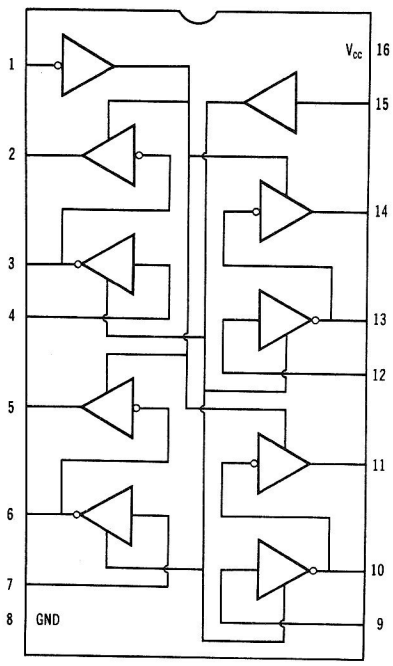

U1A,U1B,U1C,U1D,
U1E,U3B,U4B

74174



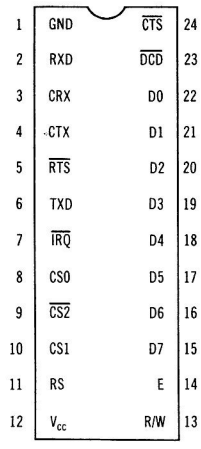

U1F

N8T26N



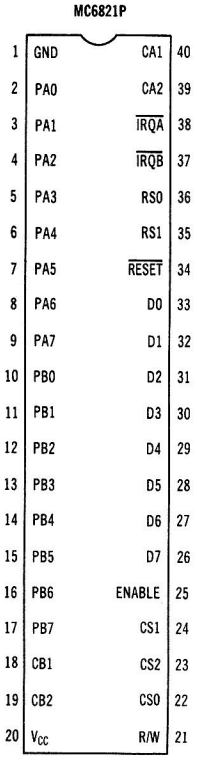

U1G,U2G

6850P



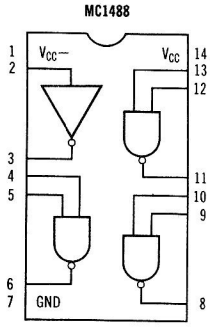

U2A,U2B,U2C,U2D,U3C

MC6821P




U2E,U2F

MC1488




U3A

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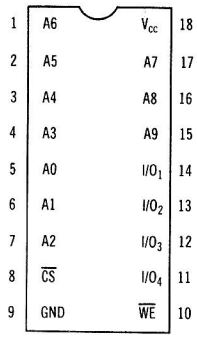
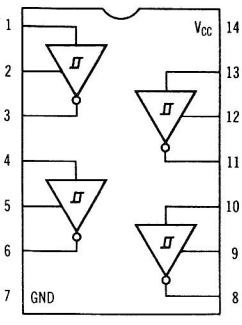
2114L



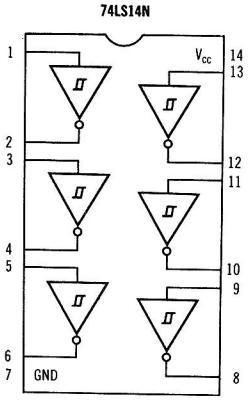

U3D,U3E,U3F,U3G
U3H,U3I,U3J,U3K
U4C,U4D,U4E,U4F
U4G,U4H,U4I,U4

SN75189N



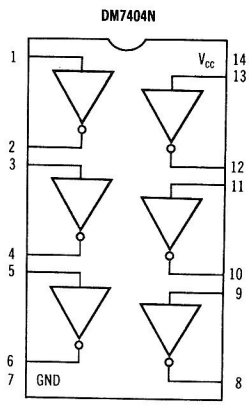

U4A

74LS14N




U5B,U7A

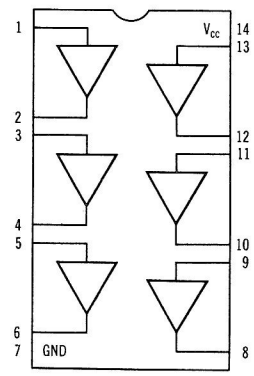
DM7404N




U5C,U5D,U5H,U6A
U6H,U6J,U7J

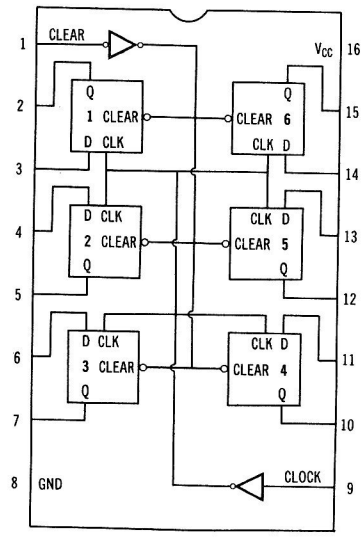
# 555 BOARD PINOUTS

F7417PC




U1A,U1B,U1C,U1D,
U1E,U3B,U4B

74174

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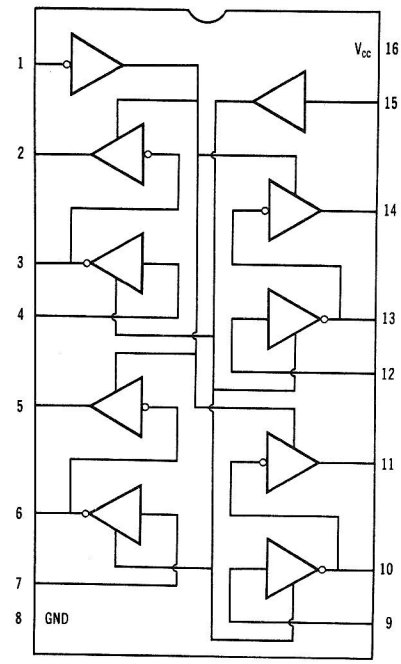
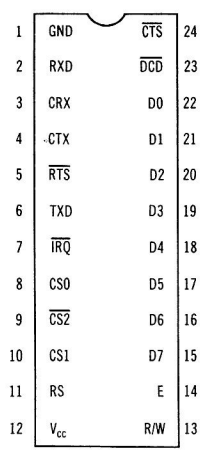


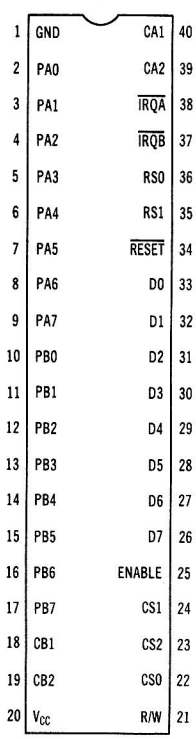

U1G,U2G

6850P



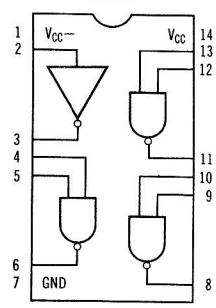

U2A,U2B,U2C,U2D,U3C

MC6821P



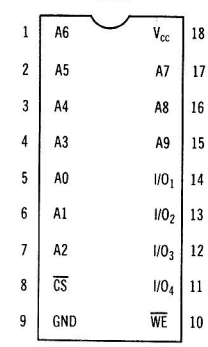

U2E,U2F

MC1488



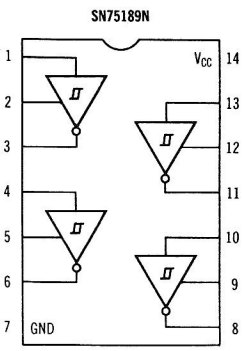

U3A

SY2114L
2114L




U3D,U3E,U3F,U3G
U3H,U3I,U3J,U3K
U4C,U4D,U4E,U4F
U4G,U4H,U4I,U4

SN75189N

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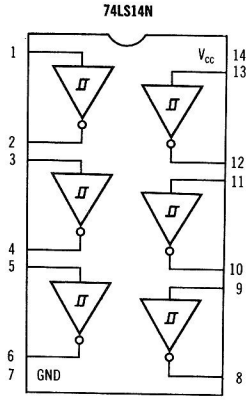
74LS14N




U5B,U7A

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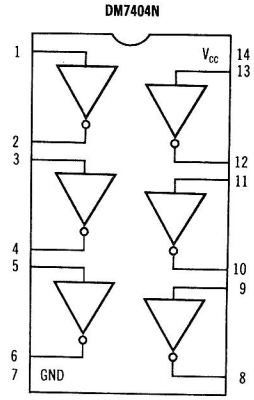
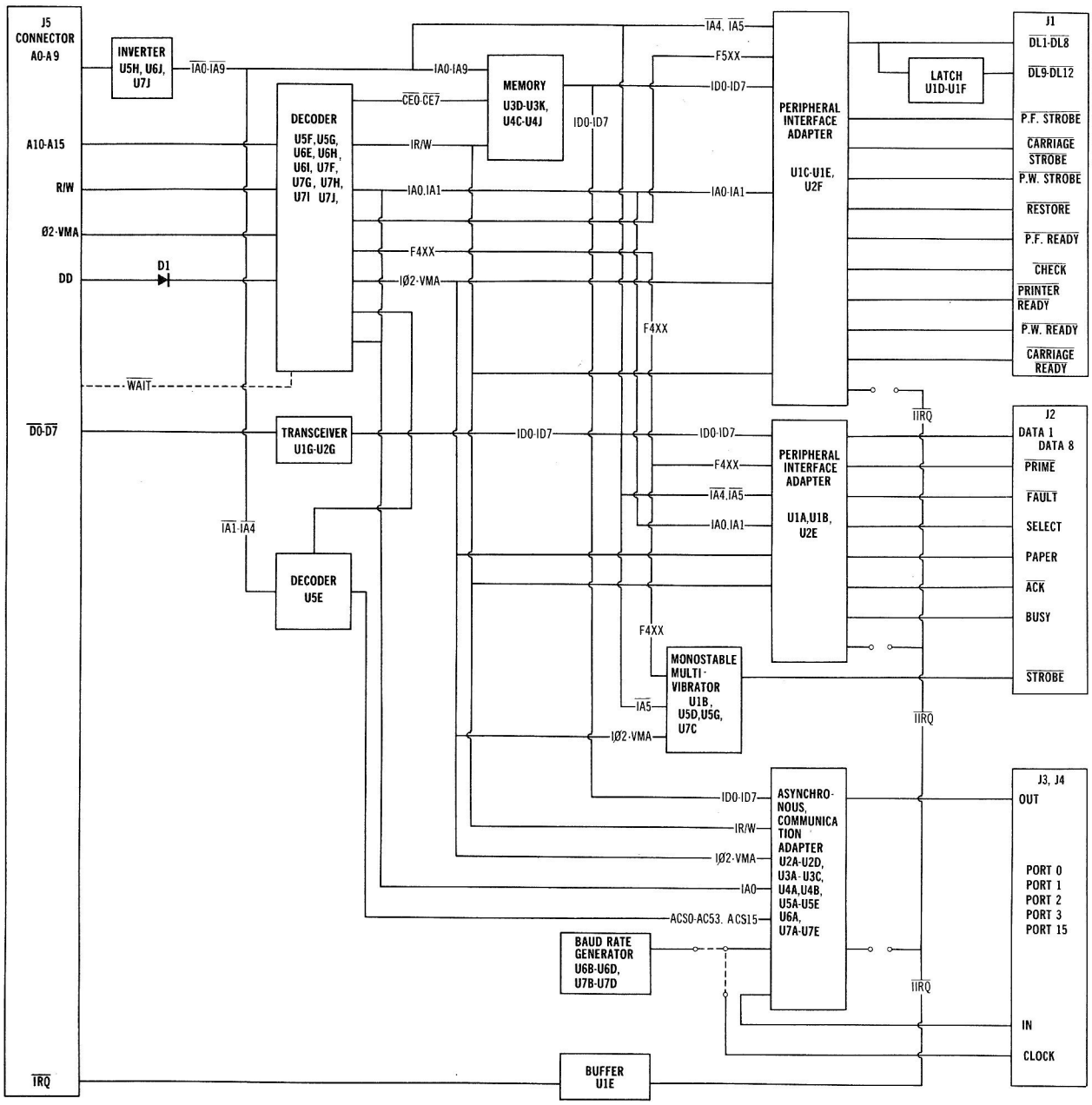
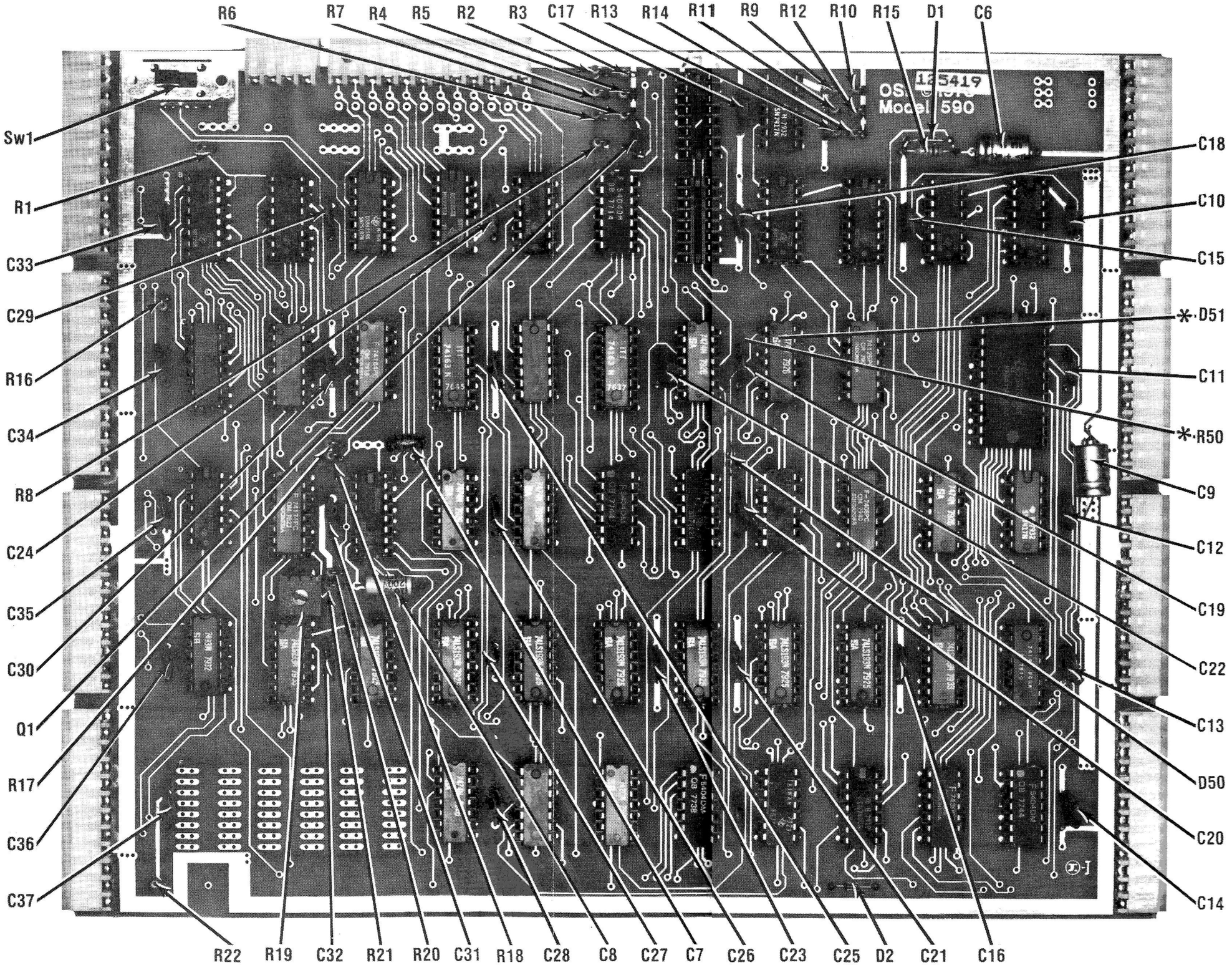



U5C,U5D,U5H,U6A
U6H,U6J,U7J

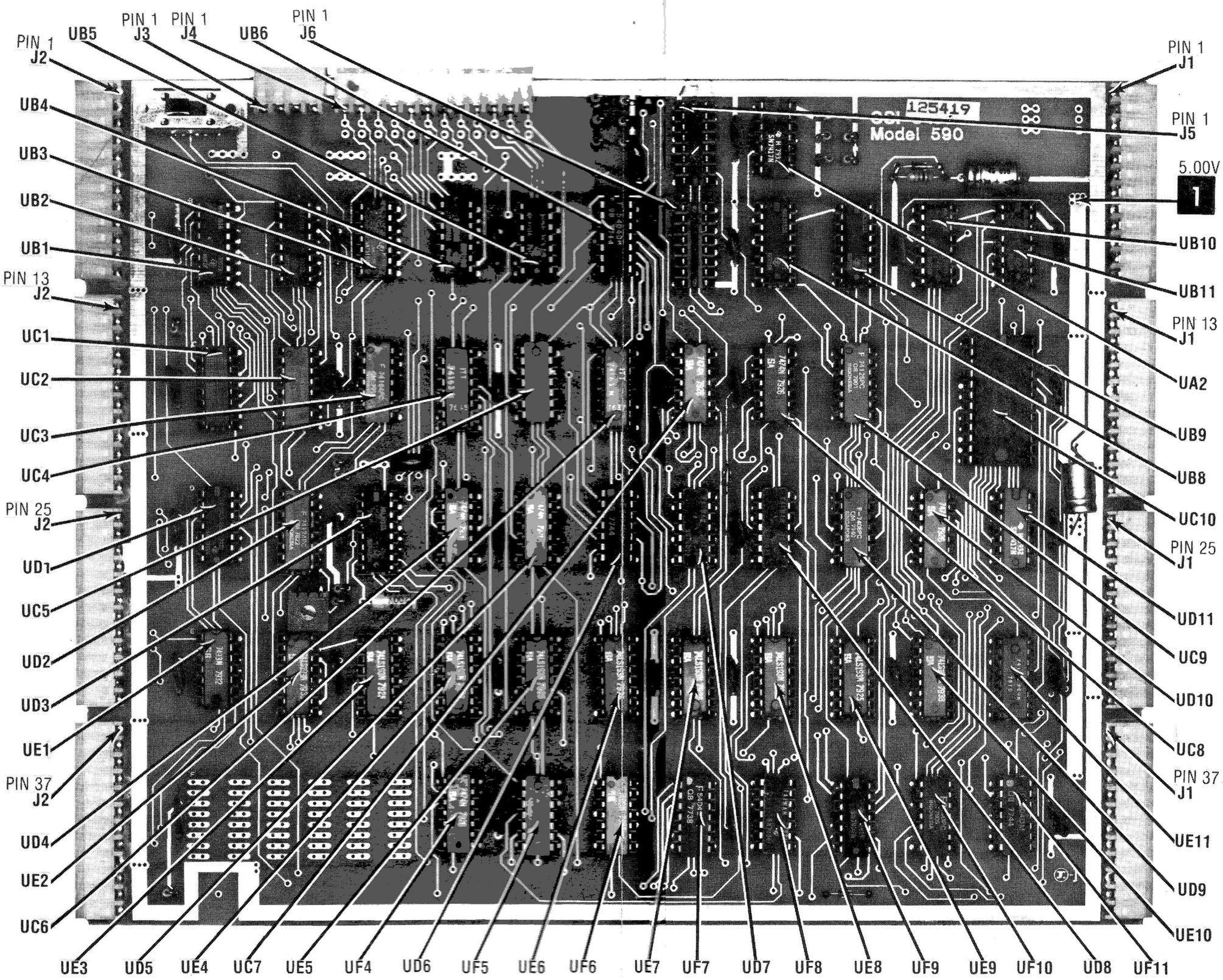



# 555 BOARD BLOCK




*LOCATED OTHER SIDE OF BOARD

**590 BOARD**




A Howard W. Sams CIRCUITRACE® Photo

590 BOARD

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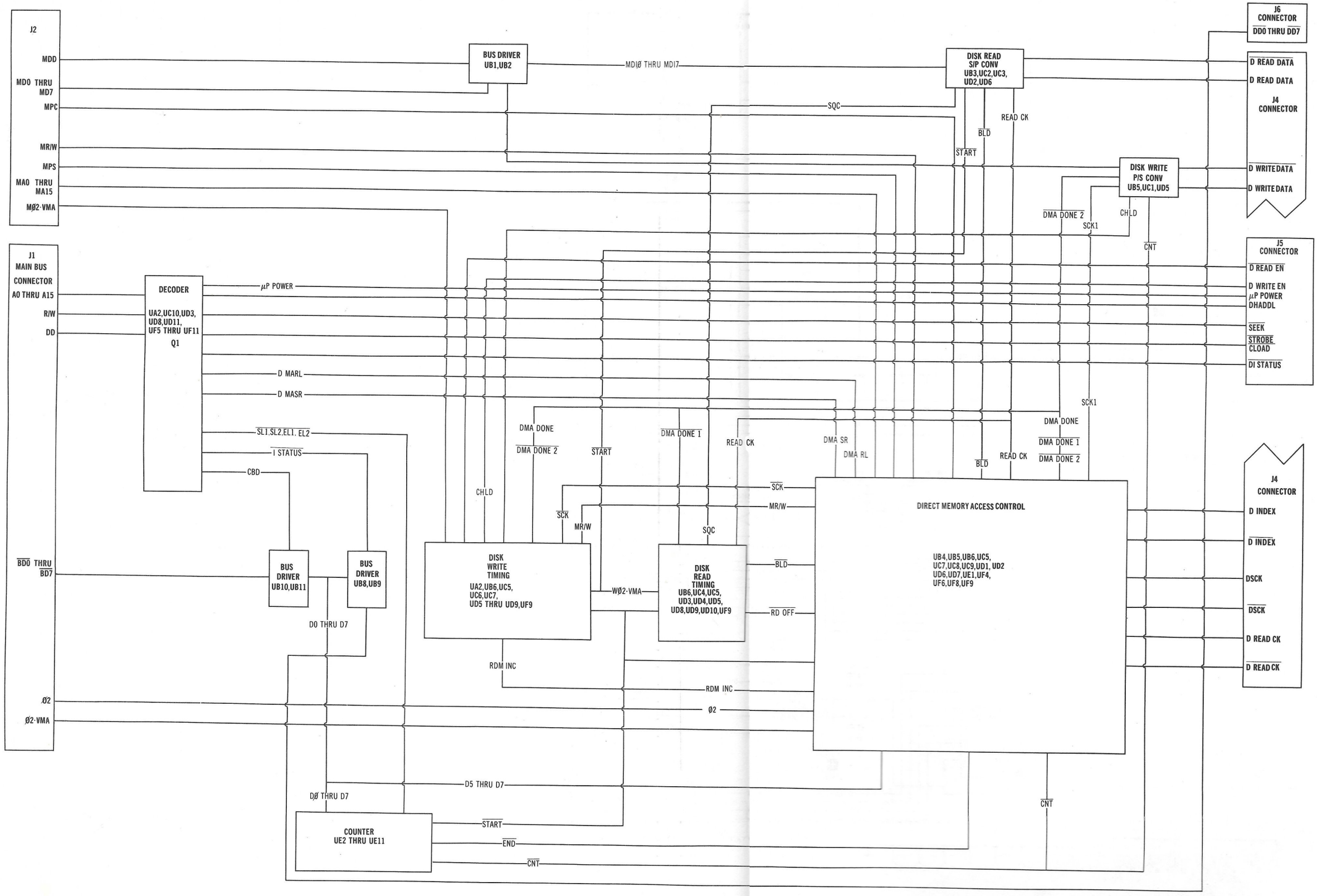
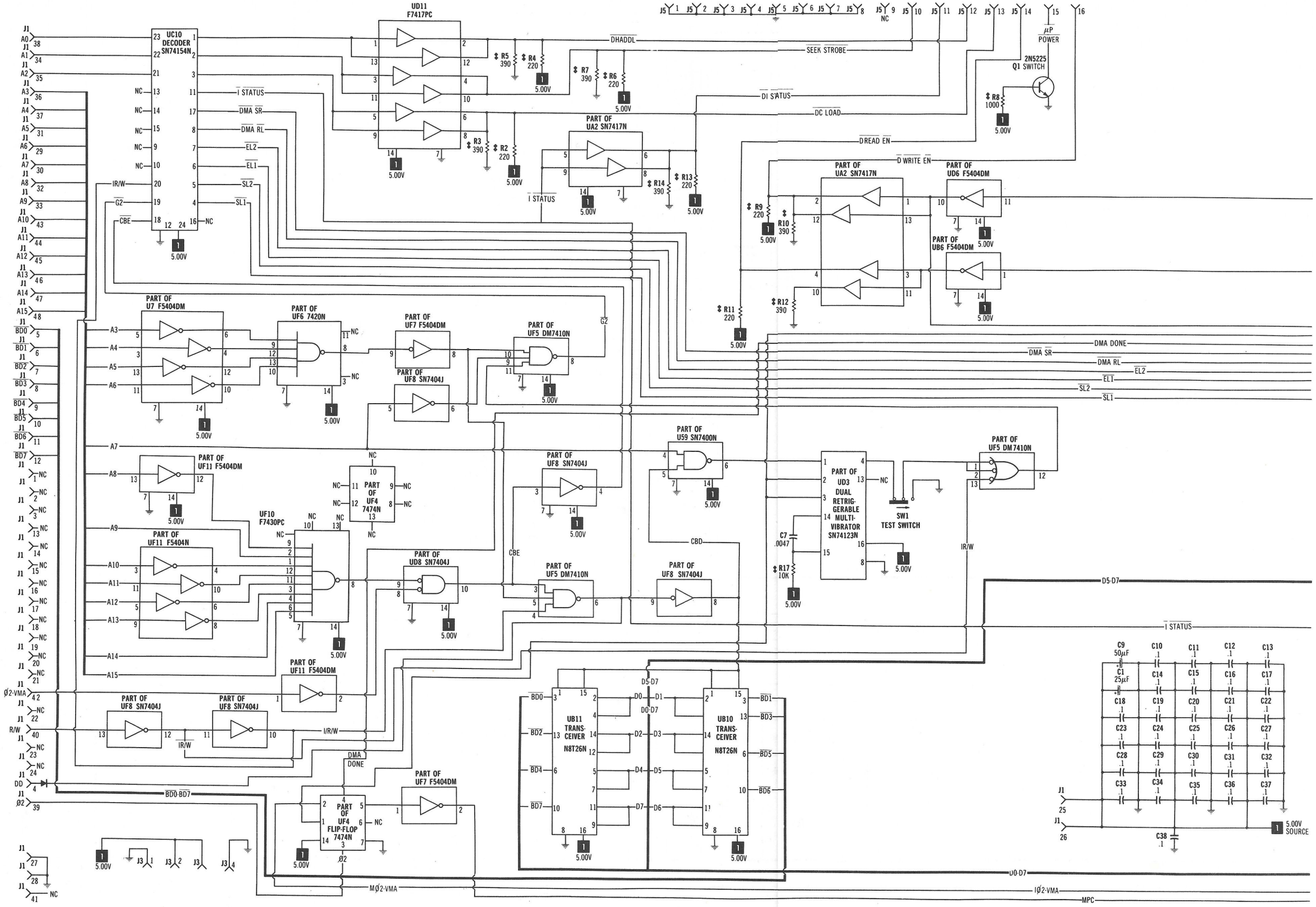
154


J2
MDD
MD0 THRU MD7
MPC
MR/W
MPS
MA0 THRU MA15
MØ2-VMA
J1 MAIN BUS CONNECTOR
A0 THRU A15
R/W
DD
BD0 THRU BD7
ØI2
Ø2-VMA
BUS DRIVER UB1,UB2
MDIØ THRU MDI7
DECODER
UA2,UC10,UD3, UD8,UD11, UF5 THRU UF11 Q1
μP POWER
D MARL
D MASR
SL1.SL2.EL1. EL2
I STATUS
CBD
BUS DRIVER UB10,UB11
BUS DRIVER UB8,UB9
D0 THRU D7
DØ THRU D7
CHLD
DMA DONE
DMA DONE 2
START
DMA DONE 1
SCK
MR/W
DISK WRITE TIMING UA2,UB6,UC5, UC6,UC7, UD5 THRU UD9,UF9
WØ2-VMA
RDM INC
DISK READ TIMING UB6,UC4,UC5, UD3,UD4,UD5, UD8,UD9,UD10,UF9
SQC
BLD
RD OFF
READ CK
DISK READ S/P CONV UB3,UC2,UC3, UD2,UD6
DISK WRITE P/S CONV UB5,UC1,UD5
DMA DONE 2
SCK1
CNT
DMA SR
DMA RL
DIRECT MEMORY ACCESS CONTROL
UB4,UB5,UB6,UC5, UC7,UC8,UC9,UD1, UD2 UD6,UD7,UE1,UF4, UF6,UF8,UF9
RDM INC
Ø2
D5 THRU D7
COUNTER UE2 THRU UE11
START
END
CNT
J6 CONNECTOR
DD0 THRU DD7
D READ DATA
D READ DATA
J4 CONNECTOR
D WRITE DATA
D WRITE DATA
J5 CONNECTOR
D READ EN
D WRITE EN
μP POWER
DHADDL
SEEK
STROBE
CLOAD
DI STATUS
J4 CONNECTOR
D INDEX
D INDEX
DSCK
DSCK
D READ CK
D READ CK



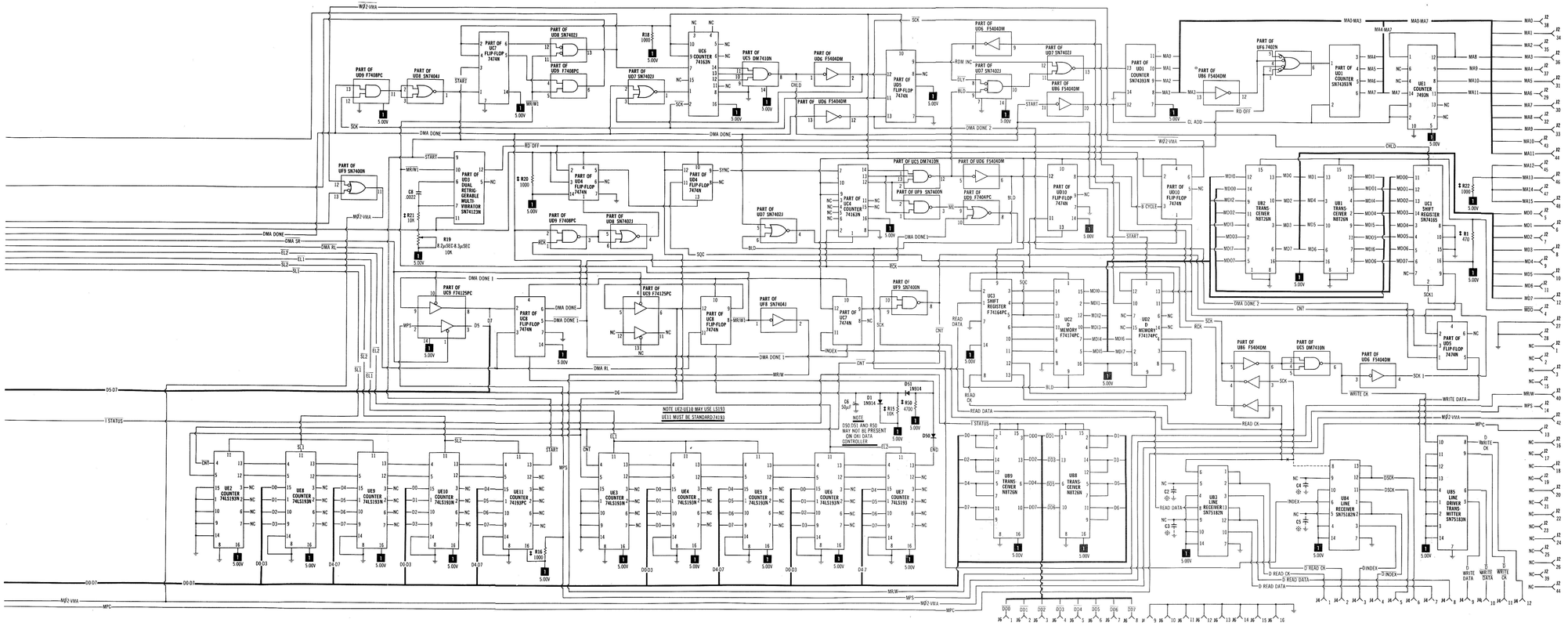

A PHOTOFACT STANDARD NOTATION SCHEMATIC WITH CIRCUITRACE®



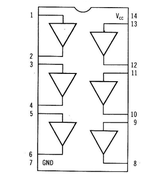
FOR SCHEMATIC LEGEND AND NOTES SEE PAGES 181, 182 & REAR COVER.

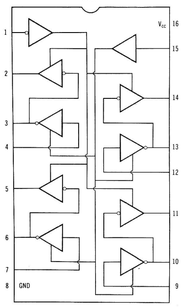


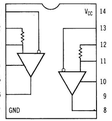
590 BOARD



## 590 BOARD PINOUTS



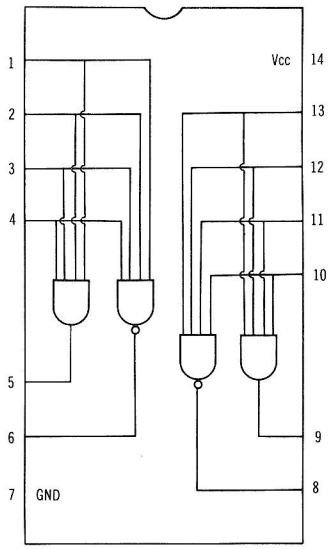





FOR SCHEMATIC LEGEND AND NOTES SEE PAGES 181, 182 & REAR COVER.

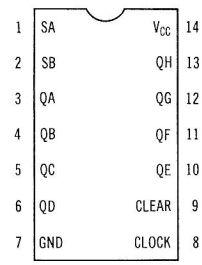
# 590 BOARD PINOUTS (CONTINUED)

SN75183N



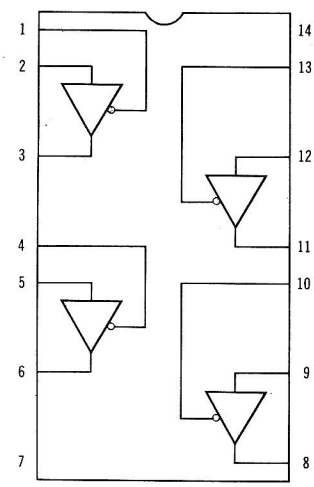

UB5

F74164PC



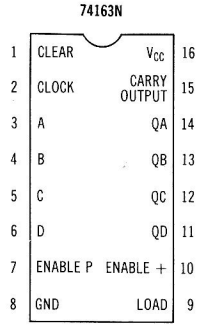

UC3

F74125PC



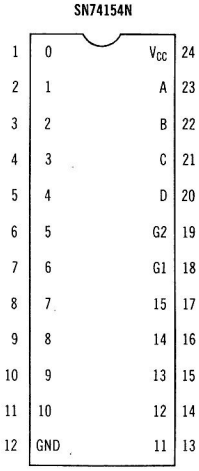

UC9

74163N



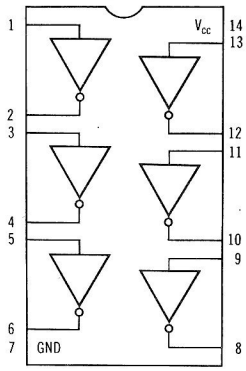

UC4,UC6

SN74154N



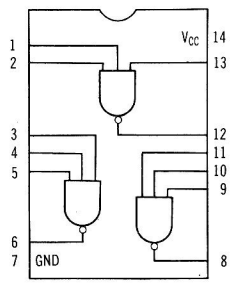

UC10

F5404DM
SN7404J



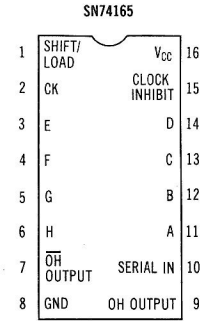

UB6,UD6,UF7,UF8,UF11

DM7410N




UC5,UF5

SN74165




UC1

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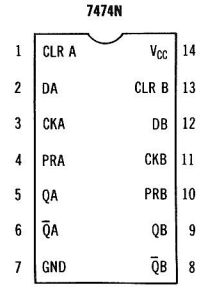
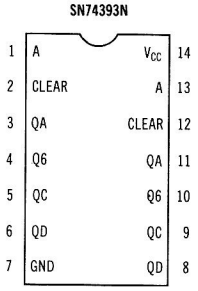



UC7,UC8,UD4,UD5,
UD10,UF4

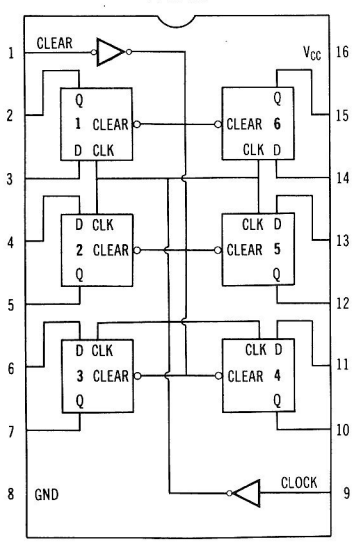
SN74393N




UD1

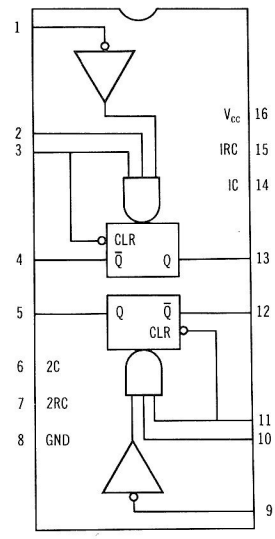
# 590 BOARD PINOUTS (CONTINUED)

F-74174PC



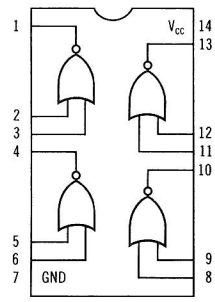

UD2,UC2

SN74123N



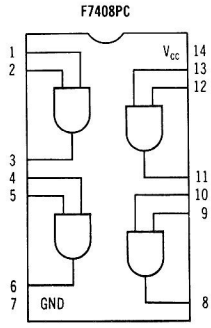

UD3

SN7402J



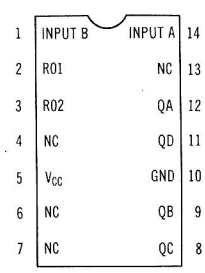

UD7,UD8

F7408PC



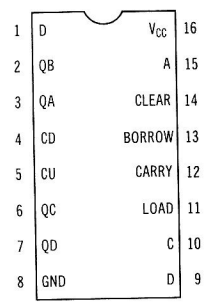

UD9

7493N



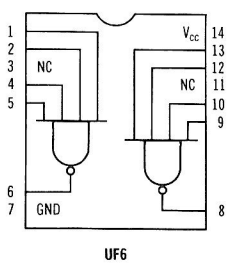

UE1

74193PC
74LS193N




UE2 THRU UE11

7420

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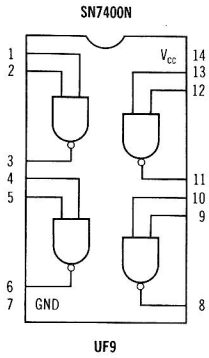


UF9

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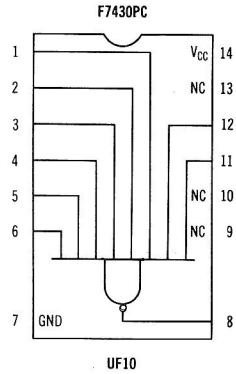
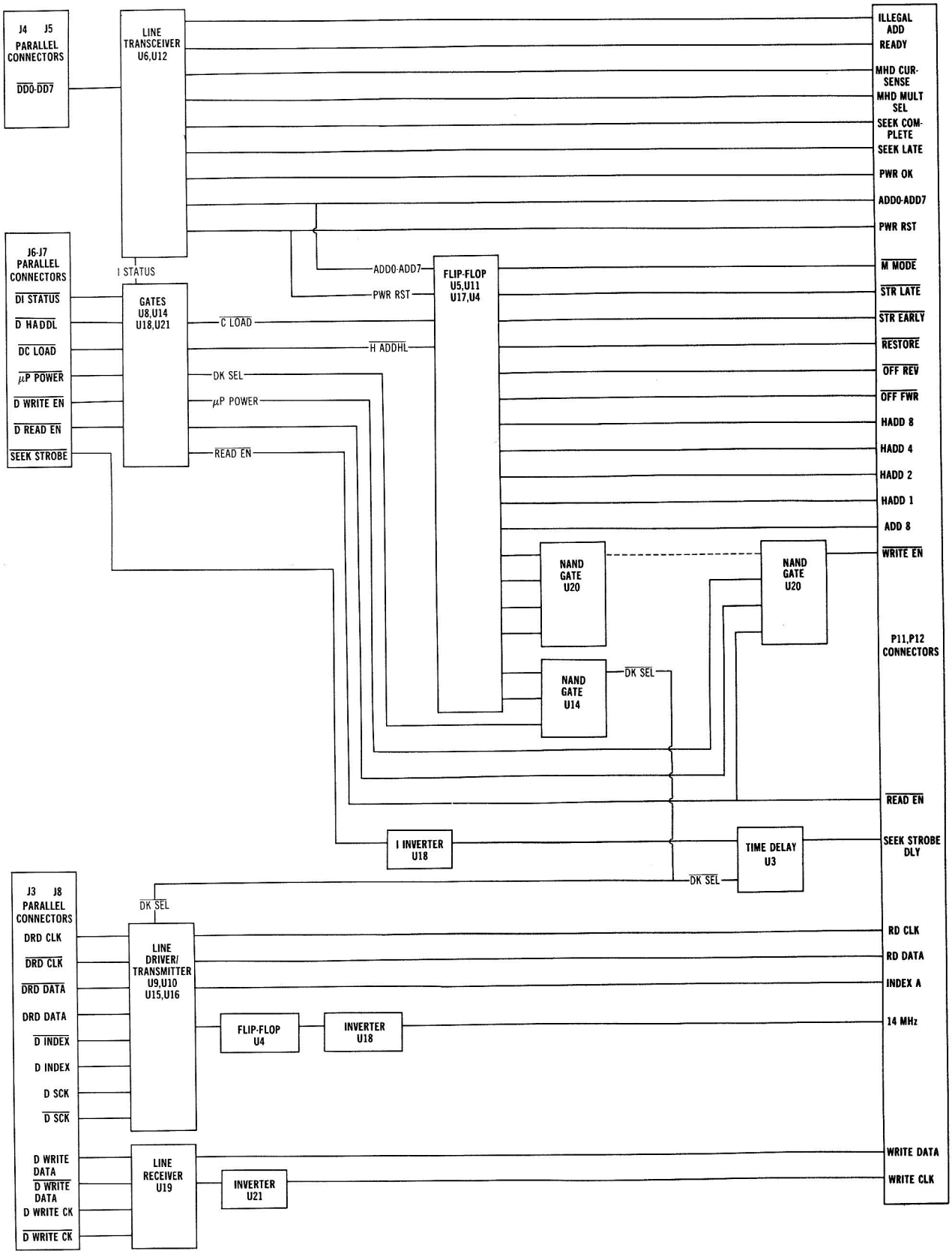



UF10

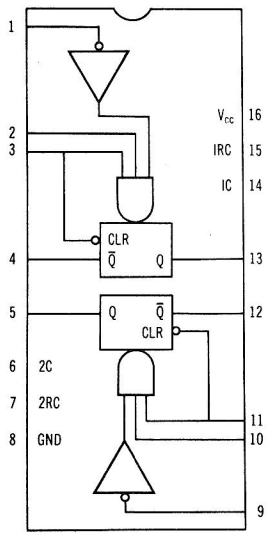

Q1




# 592 BOARD BLOCK

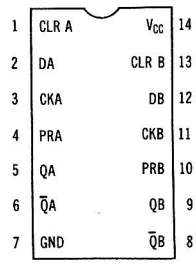
# 592 BOARD PINOUTS

SN74123N



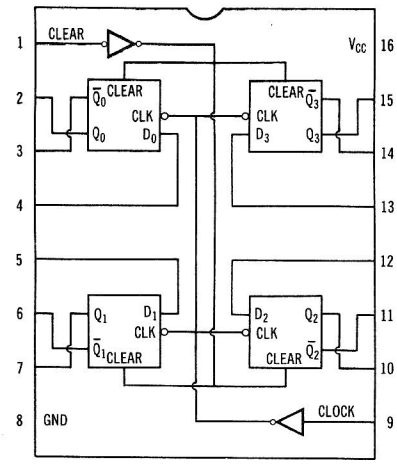

U3

SN7474N



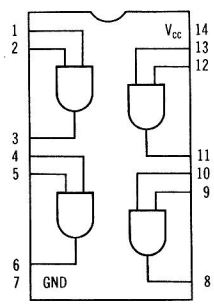

U4

DM74175N
F74175PC



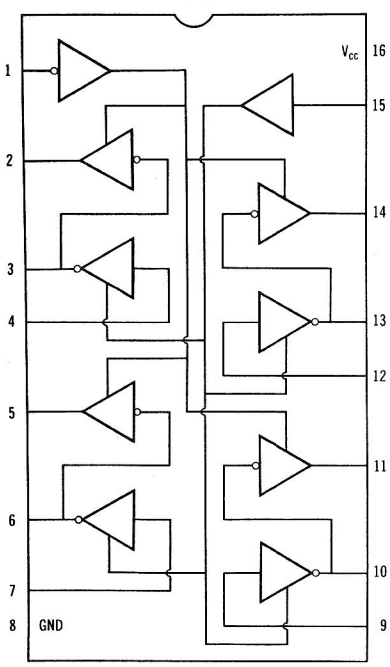

U5,U11,U17

7408N



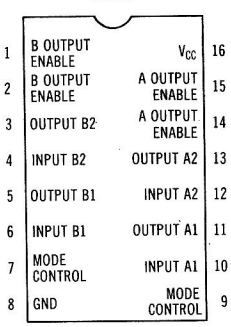

U8

N8T26AN



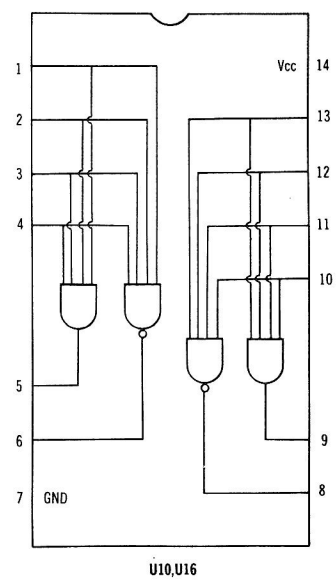

U6,U12

DS8831



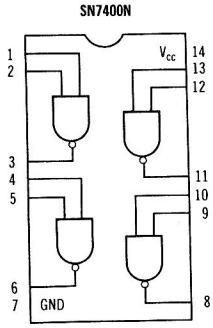

U9,U15

SN75183N



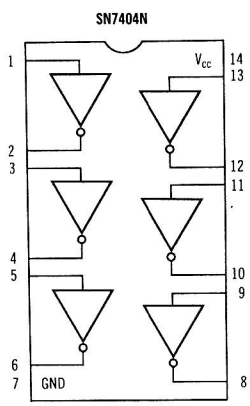

U10,U16

SN7400N



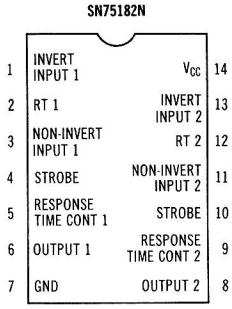

U14

SN7404N



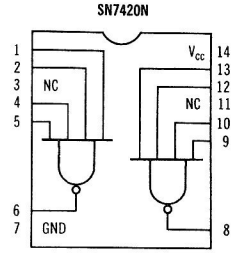

U18,U21

SN75182N

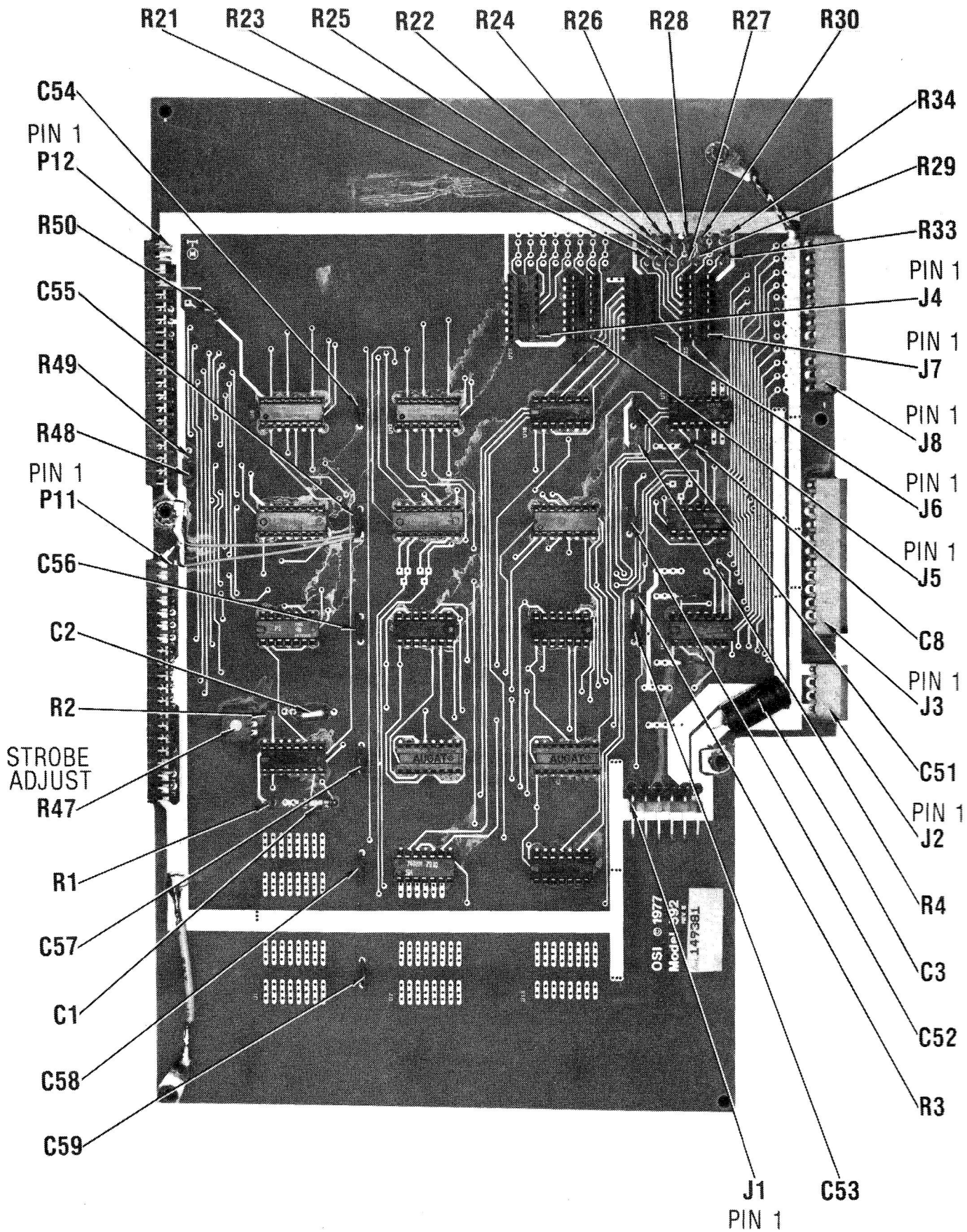



U19

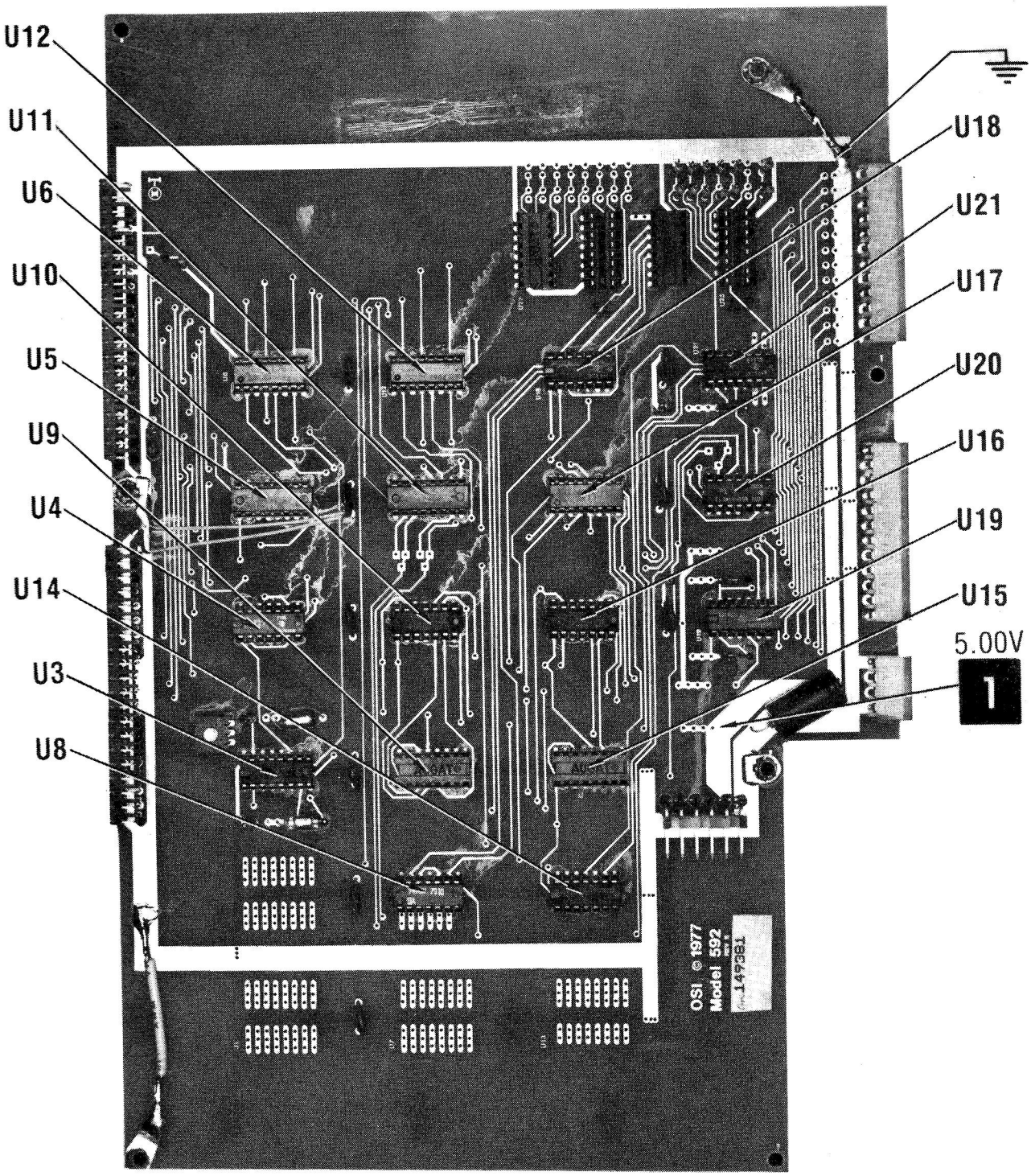
SN7420N



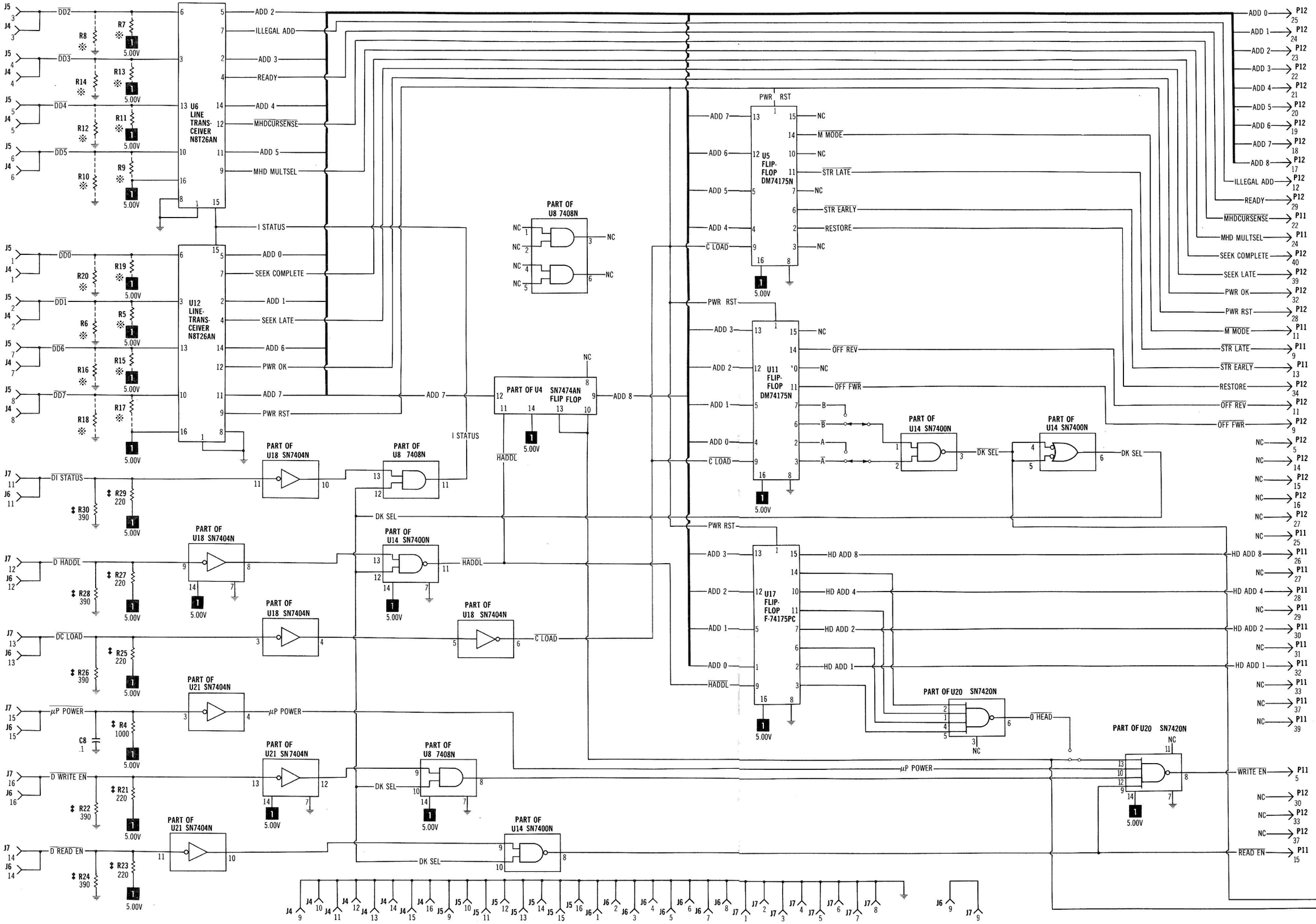

U20


R21
R23
R25
R22
R24
R26
R28
R27
R30
C54
PIN 1
P12
R50
C55
R49
R48
PIN 1
P11
C56
C2
R2
STROBE
ADJUST
R47
R1
C57
C1
C58
C59
R34
R29
R33
PIN 1
J4
PIN 1
J7
PIN 1
J8
PIN 1
J6
PIN 1
J5
C8
PIN 1
J3
C51
PIN 1
J2
R4
C3
C52
R3
J1
PIN 1
C53
OSI © 1977
Model 592

592 BOARD




**592 BOARD** A Howard W. Sams CIRCUITRACE® Photo

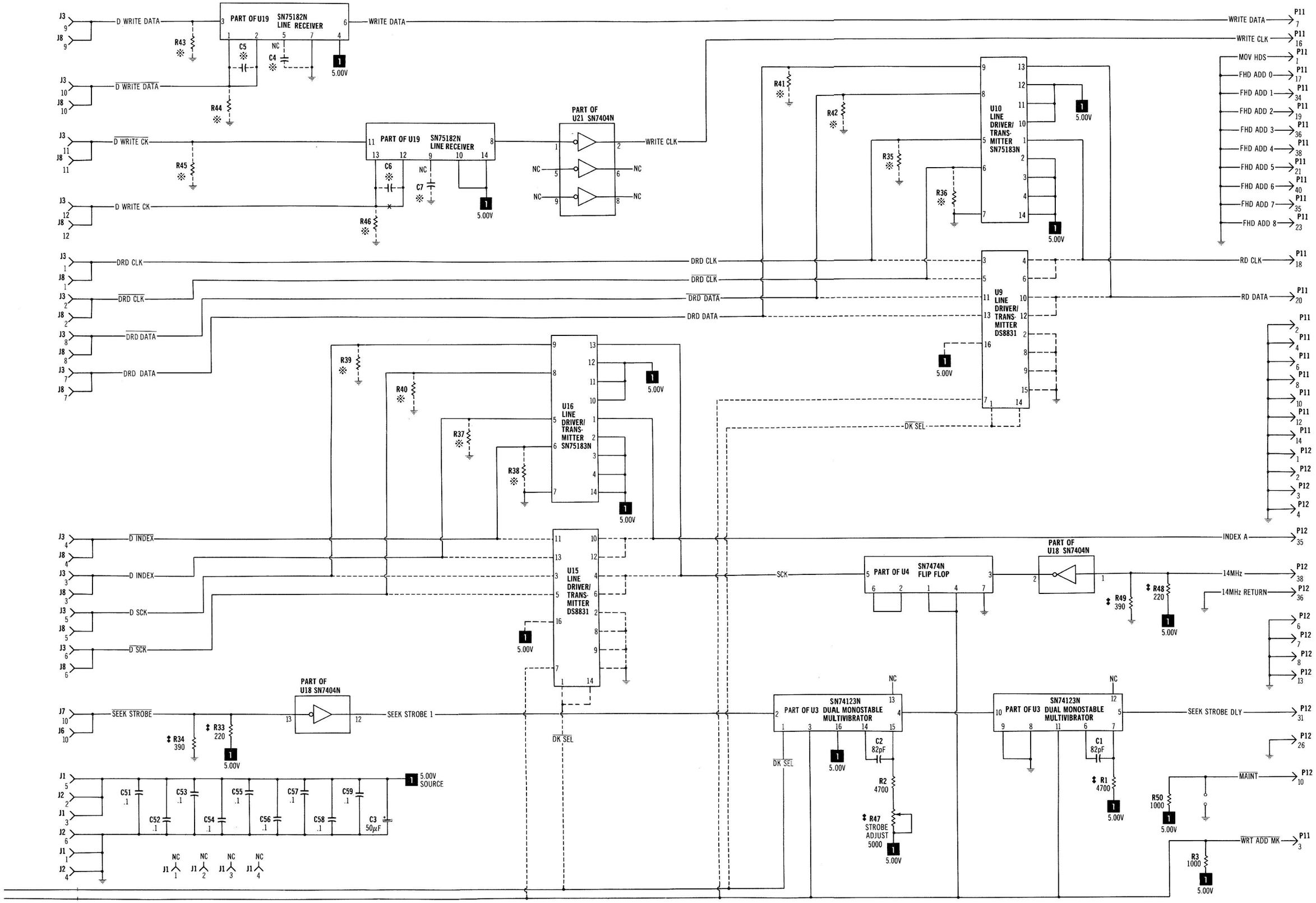


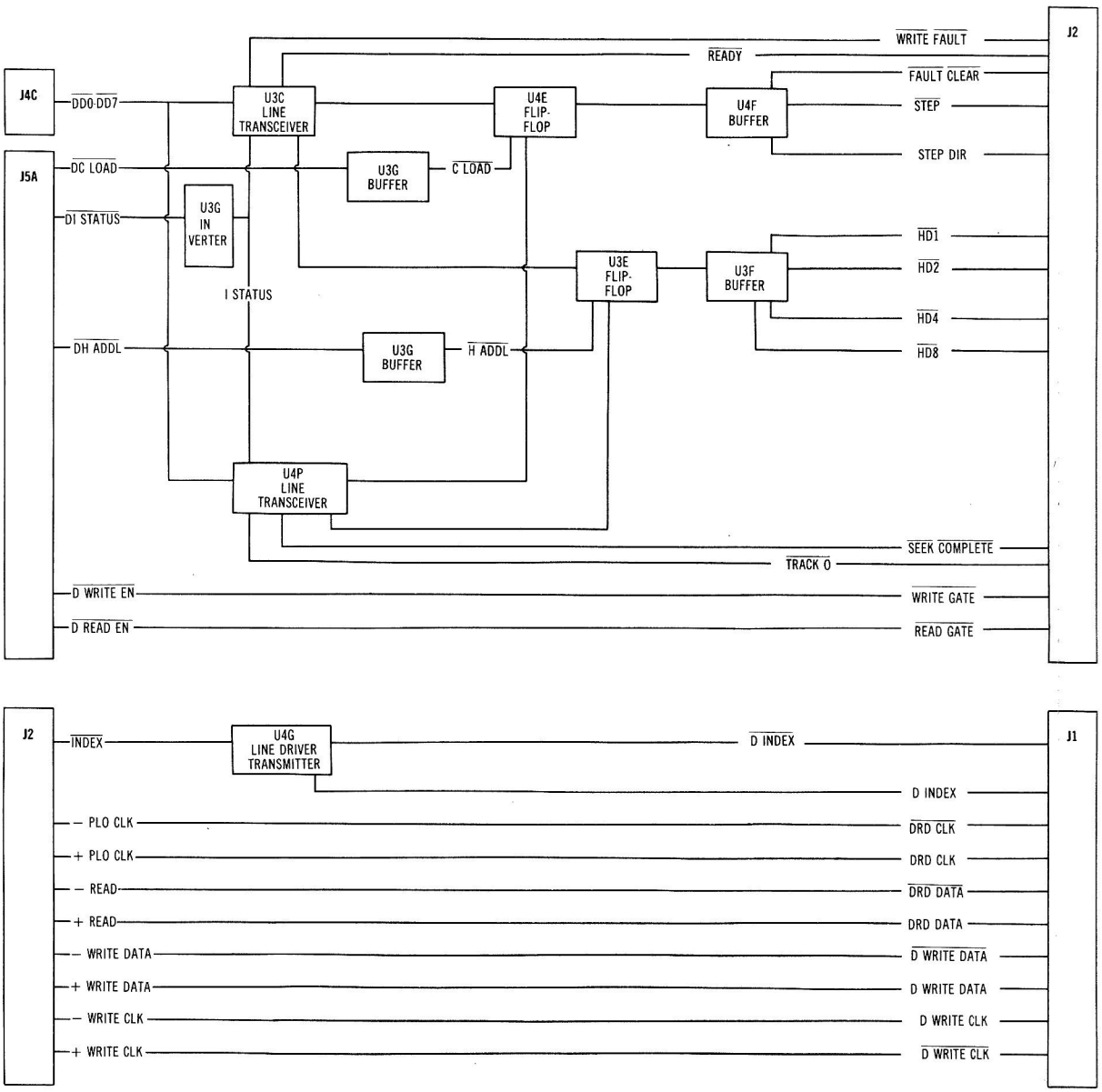

OTOFACT STANDARD NOTATION SCHEMATIC
WITH CIRCUITRACE®



## 592 BOARD

FOR SCHEMATIC LEGEND AND NOTES SEE PAGES 182 & REAR COVER.


J3 9
J8 9
D WRITE DATA
R43 ※
PART OF U19 SN75182N LINE RECEIVER
C5 ※
C4 ※
NC
5.00V
WRITE DATA
P11 7
J3 10
J8 10
D WRITE DATA
R44 ※
WRITE CLK
P11 16
J3 11
J8 11
D WRITE CK
R45 ※
PART OF U19 SN75182N LINE RECEIVER
C6 ※
C7 ※
R46 ※
PART OF U21 SN7404N
MOV HDS
P11 1
FHD ADD 0
P11 17
FHD ADD 1
P11 34
FHD ADD 2
P11 19
FHD ADD 3
P11 36
FHD ADD 4
P11 38
FHD ADD 5
P11 21
FHD ADD 6
P11 40
FHD ADD 7
P11 35
FHD ADD 8
P11 23
R41 ※
R42 ※
R35 ※
R36 ※
U10 LINE DRIVER/ TRANS- MITTER SN75183N
J3 12
J8 12
D WRITE CK
J3 1
J8 1
DRD CLK
J3 2
J8 2
DRD CLK
J3 8
J8 8
DRD DATA
J3 7
J8 7
DRD DATA
DRD CLK
DRD CLK
DRD DATA
DRD DATA
RD CLK
P11 18
RD DATA
P11 20
U9 LINE DRIVER/ TRANS- MITTER DS8831
P11 2
P11 4
P11 6
P11 8
P11 10
P11 12
P11 14
P12 1
P12 2
P12 3
P12 4
R39 ※
R40 ※
R37 ※
R38 ※
U16 LINE DRIVER/ TRANS- MITTER SN75183N
P12 5
P12 6
P12 7
P12 8
P12 13
J3 4
J8 4
D INDEX
J3 3
J8 3
D INDEX
J3 5
J8 5
D SCK
J3 6
J8 6
D SCK
U15 LINE DRIVER/ TRANS- MITTER DS8831
DK SEL
INDEX A
P12 35
SCK
PART OF U4 SN7474N FLIP FLOP
PART OF U18 SN7404N
14MHz
P12 38
14MHz RETURN
P12 36
R49 390
R48 220
J7 10
J6 10
SEEK STROBE
PART OF U18 SN7404N
SEEK STROBE 1
R34 390
R33 220
SN74123N PART OF U3 DUAL MONOSTABLE MULTIVIBRATOR
SEEK STROBE DLY
P12 31
P12 26
C2 82pF
C1 82pF
R2 4700
R1 4700
R47 STROBE ADJUST 5000
MAINT
P12 10
R50 1000
WRT ADD MK
P11 3
R3 1000
J1 5
J2 2
J1 3
J2 6
J1 1
J2 4
C51 .1
C52 .1
C53 .1
C54 .1
C55 .1
C56 .1
C57 .1
C58 .1
C59 .1
C3 50μF
5.00V SOURCE
NC J1 1
NC J1 2
NC J1 3
NC J1 4



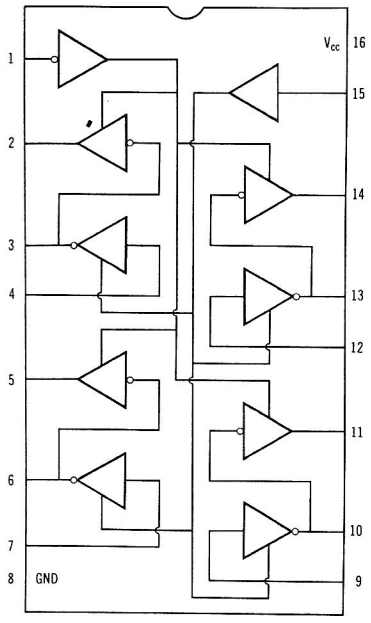




## 594 BOARD BLOCK

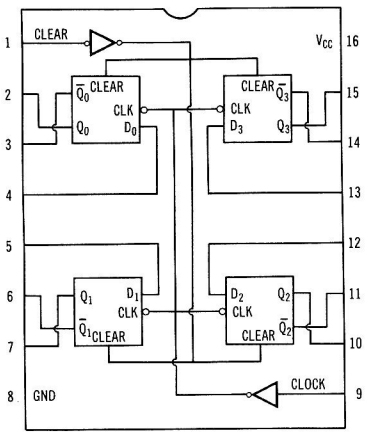
# 594 BOARD PINOUTS

N8T26N



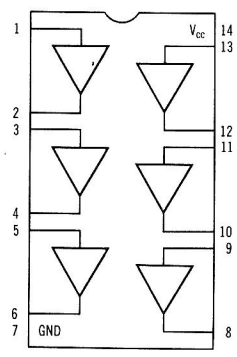

U3C,U4D

F74175PC



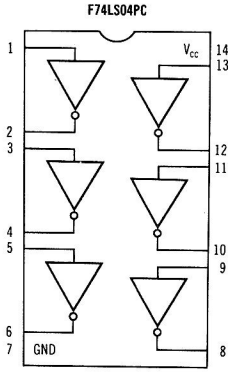

U3D,U3E,U4E

SN7417N
F7417PC



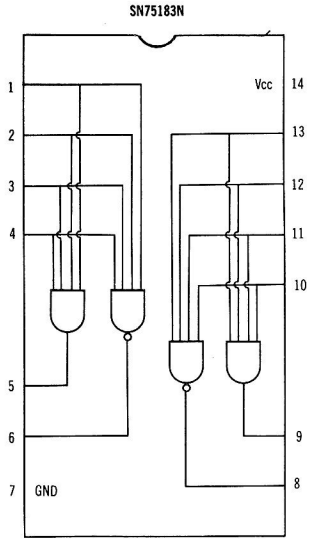

U3F,U4F

F74LS04PC

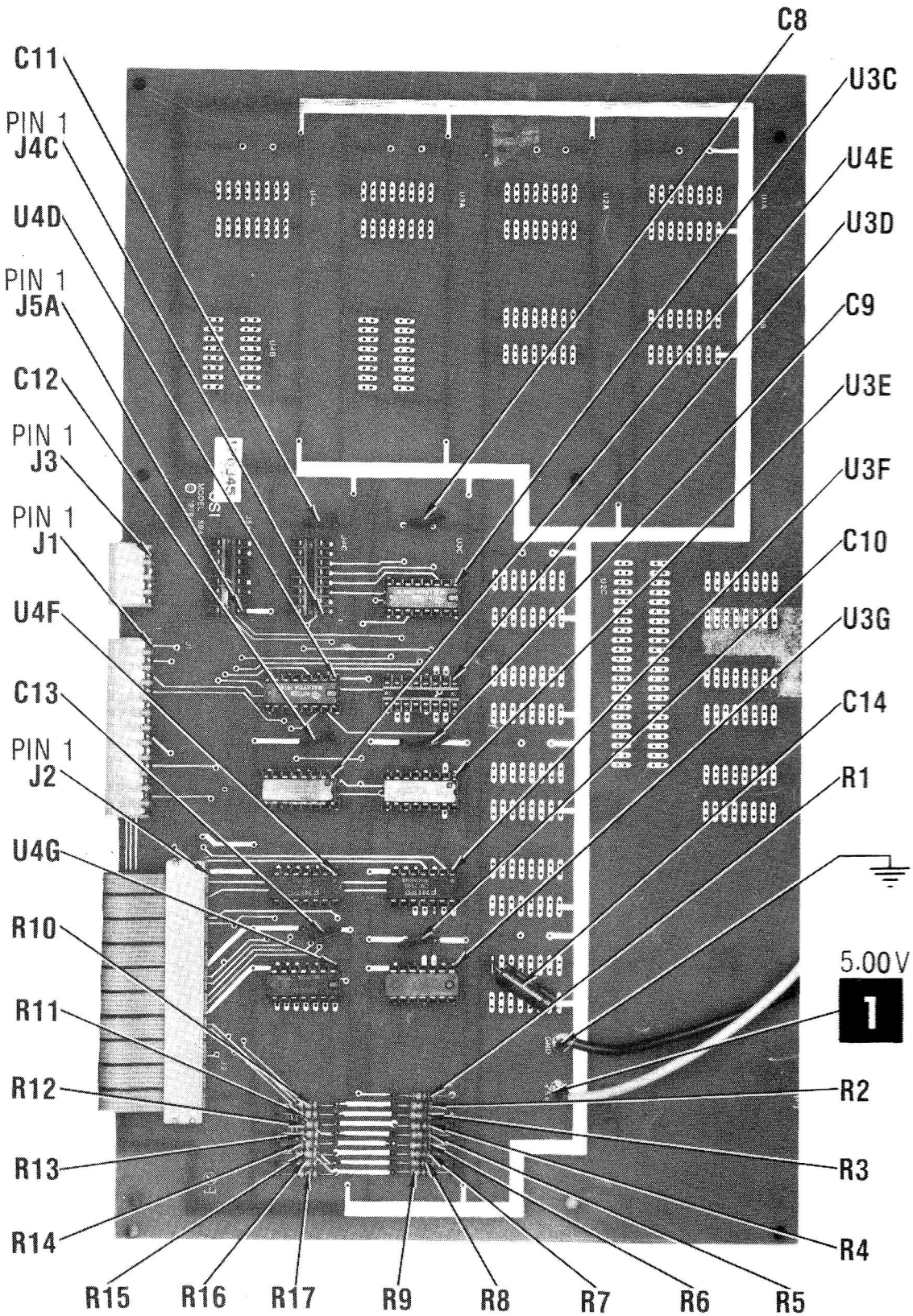



U3G

SN75183N

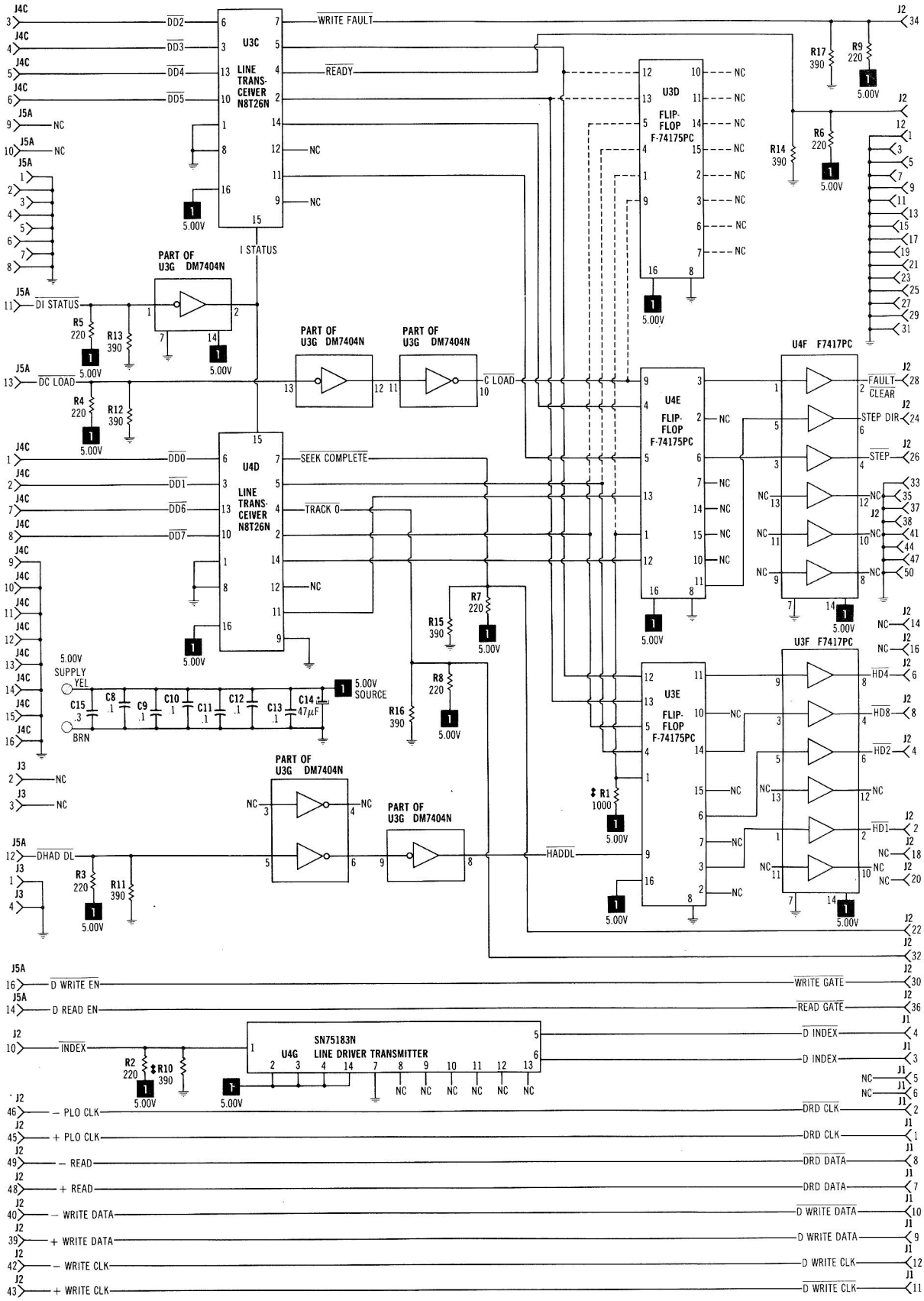



U4G




A Howard W. Sams CIRCUITRACE® Photo

**594 BOARD**




A PHOTOFACT STANDARD NOTATION SCHEMATIC
WITH CIRCUITRACE™



**594 BOARD**

**176**

**FOR SCHEMATIC LEGEND AND NOTES SEE REAR COVER.**

## LEGEND FOR 470 (FLOPPY) BOARD SCHEMATIC

**A0,A1,A2** ..... Address
**A4,A5** ..... Address
**A8-A15** ..... Address
**ACS** ..... ACIA Chip Select
**BE** ..... Board Enable
**CA1,CA2** ..... Peripheral A Interrupt Input-Control Line
**CB1,CB2** ..... Peripheral B Interrupt Input-Control Line
**CLR** ..... Clear
**DD** ..... Data Direction
**D0-D7** ..... Data
**DRIVE SELECT** ..... Drive Select
**ERASE ENABLE** ..... Erase Enable
**FAULT** ..... Fault
**FAULT RESET** ..... Fault Reset
**HEAD LOAD** ..... Head Load
**INDEX** ..... Index
**IRQ** ..... Interrupt Request
**IR/W** ..... Internal Read/Write
**IØ2·VMA** ..... Internal Phase Two· Valid Memory Address
**LOW CURRENT** ..... Low Current
**PB0-PB7** ..... Port B
**READY DRIVE 1** ..... Ready Drive One
**READY DRIVE 2** ..... Ready Drive Two
**R/W** ..... Read/Write
**SECTOR** ..... Sector
**SELECT DRIVE 1** ..... Select Drive One (Single-Sided Floppy Interface)
**SELECT DRIVE 2** ..... Select Drive Two (Single-Sided Floppy Interface)
**SEPARATED CLOCK** ..... Separated Clock
**SEPARATED DATA** ..... Separated Data
**SIDE SELECT** ..... Side Select (Dual-Sided Floppy Interface)
**STEP** ..... Step
**STEP IN** ..... Step In
**TRACK 00** ..... Track Zero

## 470 BOARD (CONTINUED)

**TX CLK** ..... Transmit Clock
**VMA** ..... Valid Memory Address
**WAIT** ..... Wait
**WRITE DATA** ..... Write Data
**WRITE ENABLE** ..... Write Enable
**WRITE PROTECT** ..... Write Protect
**Ø2·VMA** ..... Phase Two·Valid Memory Address

## LEGEND FOR 505 REV. A BOARD SCHEMATIC

**A0-A15** ..... Address
**BE** ..... Board Enable
**BRG** ..... Baud Rate Generator
**CA1** ..... Control A1
**CA2** ..... Control A2
**CB1** ..... Control B1
**CB2** ..... Control B2
**CLR** ..... Clear
**CNT** ..... Count
**$CS_D$** ..... Chip Select D
**$CS_E$** ..... Chip Select E
**$CS_F$** ..... Chip Select F
**$CS_{FL}$** ..... Chip Select Floppy Disk
**$CS_S$** ..... Chip Select Serial
**D0-D7** ..... Data
**DD** ..... Data Direct
**ERASE ENABLE** ..... Erase Enable
**FAULT** ..... Fault
**FAULT RESET** ..... Fault Reset
**HEAD LOAD** ..... Head Load
**INDEX** ..... Index
**IRQ** ..... Interrupt Request
**IR/W** ..... Internal Read/Write
**IØ2·VMA** ..... Internal Phase Two·Valid Memory Address
**LOW CURRENT** ..... Low Current

Any $\overline{\text{Bar}}$ above any alphabetical or numerical combination indicates line active in a low (0) state.

## 505 BOARD (CONTINUED)

NMI.....Non-Maskable Interrupt
PA0-PA7.....Port A
PB0-PB7.....Port B
READY DRIVE 1.....Ready Drive One
READY DRIVE 2.....Ready Drive Two
RES.....Reset
R/W.....Read/Write
SECTOR.....Sector
SELECT DRIVE 1.....Select Drive One
SELECT DRIVE 2.....Select Drive Two
SEP DATA.....Separated Data
SEP CLOCK.....Separated Clock
STEP.....Step
STEP IN.....Step In
TRACK 00.....Track Zero
TX CLK.....Transmit Clock
VMA.....Valid Memory Address
WRITE DATA.....Write Data
WRITE ENABLE.....Write Enable
WRITE PROTECT.....Write Protect
Ø0.....Phase Zero
Ø2.....Phase Two
Ø2•VMA.....Phase Two•Valid Memory Address

## LEGEND FOR 510 REV. C BOARD SCHEMATIC

A0-A19.....Address
BØ2.....Buffer Phase Two
$BE_A$.....Bus Enable (Processor 6502)
$BE_B$.....Bus Enable (Processor 6800)
CLK.....Clock
$CS1_A$.....6502 Rom Chip Select
$CS1_B$.....6800 Rom Chip Select
$CS2_A$.....6502 Rom Chip Select
$CS2_B$.....6800 Rom Chip Select
D0-D7.....Data

## 510 BOARD (CONTINUED)

DD.....Data Direct
F7XX.....Address $F7XX_{16}$
FCXX.....Address $FCXX_{16}$
FDXX.....Address $FDXX_{16}$
FEXX.....Address $FEXX_{16}$
$FFXX_A$.....Address FFXX(6502)
$FFXX_B$.....Address FFXX(6800)
HSCK1.....High Speed Clock One
HIS.....High Speed
ID0-ID7.....Internal Data
IDD.....Internal Data Direct
IIRQ.....Internal Interrupt Request
INMI...Internal Non-maskable Interrupt
IRQ.....Interrupt Request
IR/W.....Internal Read/Write
IØ2•VMA.....Internal Phase Two•Valid Memory Address
MA8-MA10.....Memory Address
$MREQ_C$.....Memory Request
NMI.....Non-maskable Interrupt
P1-P22.....Port
$PC_{H1}$.....Processor Select High
$PC_{LO}$.....Processor Select Low
PIA RESET.....Peripheral Interface Adapter Reset
PS.....Processor Select
$PS_A$.....6502 Select
$PS_B$.....6800 Select
$PS_C$.....Z-80 Select
RAMCE.....Random Access Memory Chip Enable
RD.....Z80 Read
RDY.....Ready
$RE_A$.....Read Enable(6502)
$RE_B$.....Read Enable(6800)
RES.....Reset
$RFSH_C$.....Refresh
RS.....Ram Select
R/W.....Read/Write

Any $\overline{\text{Bar}}$ above any alphabetical or numerical combination indicates line active in a low (0) state.

## 510 BOARD (CONTINUED)

RX ..... Receive Data
RX CLK ..... Receive Clock
TX CLK ..... Transmit Clock
VMA ..... Valid Memory Address
WAIT ..... Wait
WR ..... Z80 Write
$\phi 1_B$ ..... Phase One(6800)
$\phi 2$ ..... Phase Two
$\phi 2_A$ ..... Phase Two(6502)
$\phi 2_B$ ..... Phase Two(6800)
$\phi 2 \cdot VMA$ ..... Phase Two•Valid Memory Address

## LEGEND FOR 520 REV. B BOARD SCHEMATIC

A0-A17 ..... Address
CE0-CE3 ..... Chip Enable
D0-D7 ..... Data
DD ..... Data Direction
DI0-DI7 ..... Data In
DO0-DO7 ..... Data Out
R/W ..... Read/Write
WAIT ..... Wait
$\phi 2 \cdot VMA$ ..... Phase Two • Valid Memory Address

## LEGEND FOR 520 REV. C BOARD SCHEMATIC

A0-A19 ..... Address
MA0-MA11 ..... Memory Address
D0-D7 ..... Data
CE0-CE3 ..... Chip Enable
DD ..... Data Direct
R/W ..... Read/Write
MR/W ..... Memory Read/Write

## 520 BOARD (CONTINUED)

DI0-DI7 ..... Data In
DO0-DO7 ..... Data Out
WAIT ..... Wait
$\phi 2 \cdot VMA$ ..... Phase Two•Valid Memory Address

## LEGEND FOR 525 BOARD SCHEMATIC

BA0-BA19 ..... Backplane Address
BD0-BD7 ..... Backplane Data
BBE ..... Backplane Bus Enable
BIE ..... Backplane Input Enable
BR/W ..... Backplane Read/Write
B$\phi$2 VMA ... Backplane Phase Two•Valid Memory Address
CA0-CA19 ..... Port Address
CBE ..... Port Bus Enable
CD0-CD7 ..... Port Data
CE0-CE15 ..... Chip Enable For RAM
CIE ..... Port Input Enable
CR/W ..... Port Read/Write
C$\phi$2 VMA ..... Port Phase Two•Valid Memory Address
$DD_B$ ..... Data Direct Backplane
$DD_P$ ..... Data Direct Port
MA0-MA13 ..... Memory Address
MD0-MD7 ..... Memory Data
MR/W ..... Memory Read/Write
PC ..... Port Control
PS ..... Port Status
$WAIT_B$ ..... Wait Backplane
$WAIT_P$ ..... Wait Port

## LEGEND FOR 527 BOARD SCHEMATIC

A0-A19 ..... Address
CE0-CE23 ..... Chip Enable RAM

Any $\overline{\text{Bar}}$ above any alphabetical or numerical combination indicates line active in a low (0) state.

## 527 BOARD (CONTINUED)

DD ..... Data Direct
DO-D7 ..... Data
IR/W ..... Internal Read/Write
MM ..... Memory Management
R/W ..... Read/Write
VMA ..... Valid Memory Address
WAIT ..... Wait
YO-Y1-Y2 ..... Upper Memory Decode
ØO ..... Phase Zero
Ø2·VMA ..... Phase Two · Valid Memory Address

## LEGEND FOR 535 BOARD SCHEMATIC

AO-A19 ..... Address
BE ..... Bus Enable
DO-D7 ..... Data
DD ..... Data Direct
DIO-DI7 ..... Data In
DL1-DL16 ..... Delay
DOO-DO7 ..... Data Out
E2 ..... Enable Two
IØ2 ..... Internal Phase Two
IR/W ..... Internal Read/Write
MAO-MA6 ..... Memory Address
RASO-RAS2 ..... Row Address Strobe
RE ..... Row Enable
R/W ..... Read/Write
ØOIN ..... Phase Zero In
Ø2 ..... Phase Two
Ø2·VMA ..... Phase Two·Valid Memory Address
ØDETECT ..... Phase Detect

## LEGEND FOR 550 BOARD SCHEMATIC

AO ..... Address Zero
A1-A4 ..... Address

## 550 BOARD (CONTINUED)

A8-A19 ..... Internal Data
BE ..... Bus Enable
BRG ..... Baud Rate Generator
CS1-CS16 ..... Chip Select
DO-D7 ..... Data
DD ..... Data Direct
DE ..... Data Enable
IAO ..... Internal Address Zero
IDO-ID7 ..... Internal Data
IRQ ..... Interrupt Request
IR/W ..... Internal Read/Write
IØ2·VMA ..... Internal Phase Two·Valid Memory Address
R/W ..... Read/Write
SPR-I ..... Spare In
SPR-O ..... Spare Out
WAIT ..... Wait
Ø2·VMA ..... Phase Two·Valid Memory Address

## LEGEND FOR 555 BOARD SCHEMATIC

AO-A15 ..... Address
ACK ..... Acknowledge
ACSO-ACS3 ..... ACIA Chip Select
ACS15 ..... ACIA Chip Select
BUSY ..... Busy
CARRIAGE READY ..... Carriage Ready
CARRIAGE STROBE ..... Carriage Strobe
CEO-CE7 ..... Chip Enable
CHECK ..... Check
DATA 1-DATA 8 ..... Data Lines (Centronics Interface)
DO-D7 ..... Data
DD ..... Data Direct
DL1-DL12 ..... Data Line (NEC Interface)
FAULT ..... Fault
F4XX ..... Address $F4XX_{16}$

Any $\overline{\text{Bar}}$ above any alphabetical or numerical combination indicates line active in a low (0) state.

## 555 BOARD (CONTINUED)

F5XX ..... Address $F5XX_{16}$
IA0-IA9 ..... Internal Address
ID0-ID7 ..... Internal Data
IIRQ ..... Internal Interrupt Request
IRQ ..... Interrupt Request
IR/W ..... Internal Read/Write
IØ2•VMA ..... Internal Phase Two•Valid Memory Address
PAPER ..... Paper
P.F. READY ..... Paper Feed Ready
P.F.STROBE ..... Paper Feed Strobe
PORT 0 CLOCK ..... Port 0 Clock
PORT 0 IN ..... Port 0 In
PORT 0 OUT ..... Port 0 Out
PORT 1 CLOCK ..... Port 1 Clock
PORT 1 IN ..... Port 1 In
PORT 1 OUT ..... Port 1 Out
PORT 2 CLOCK ..... Port 2 Clock
PORT 2 IN ..... Port 2 In
PORT 2 OUT ..... Port 2 Out
PORT 3 CLOCK ..... Port 3 Clock
PORT 3 IN ..... Port 3 In
PORT 3 OUT ..... Port 3 Out
PORT 15 CLOCK ..... Port 15 Clock
PORT 15 IN ..... Port 15 In
PORT 15 OUT ..... Port 15 Out
PRIME ..... Prime
PRINTER READY ..... Printer Ready
P.W. READY ..... Print Wheel Ready
P.W. STROBE ..... Print Wheel Strobe
RESTORE ..... Restore
R/W ..... Read/Write
SELECT ..... Select
STROBE ..... Strobe
WAIT ..... Wait
Ø2•VMA ..... Phase Two•Valid Memory Address

## LEGEND FOR 590 BOARD SCHEMATIC

A0-A15 ..... Address
B CYCLE ..... Byte Cycle
BD0-BD7 ..... Bus Data
BLD ..... Byte Load
CBD ..... Computer Bus Direction
CBE ..... Computer Bus Enable
CHLD ..... Character Load
CL ADD ..... Clear Address
CNT ..... Count
DC LOAD ..... Disk Control Load
DD ..... Data Direction
D0-D7 ..... Data
DD0-DD7 ..... Disk Data
D HADDL ..... Disk Head Address Load
D INDEX ..... Disk Index
DI STATUS ..... Disk Input Status
DLY ..... Delay
DMA DONE .. Direct Memory Access Done
DMA DONE 1 ..... Direct Memory Access Done One
DMA DONE 2 ..... Direct Memory Access Done Two
DMA RL ..... Direct Memory Access Register Load
DMA SR ..... Direct Memory Access Status Register
D READ CK ..... Disk Read Clock
D READ DATA ..... Disk Read Data
D READ EN ..... Disk Read Enable
D SCK ..... Disk Servo Clock
D WRITE CK ..... Disk Write Clock
D WRITE DATA ..... Disk Write Data
D WRITE EN ..... Disk Write Enable
EL1 ..... End Load One
EL2 ..... End Load Two
END ..... End
G2 ..... Gate Two

Any $\overline{\text{Bar}}$ above any alphabetical or numerical combination indicates line active in a low (0) state.

## 590 BOARD (CONTINUED)

INDEX ..... Index
IR/W ..... Internal Read/Write
I STATUS ..... Input Status
MD0-MD7 ..... Memory Data
MA0-MA15 ..... Memory Address
MDD ..... Memory Data Direction
MDI0-MDI7 ..... Memory Data In
MDO0-MDO7 ..... Memory Data Out
MPC ..... Memory Process Clear
MPS ..... Memory Process Set
MR/W ..... Memory Read/Write
MR/W1 ..... Memory Read/Write One
ME ..... Memory Enable
MØ2·VMA ..... Memory Phase Two·Valid Memory Address
PD ..... Partial Decode
RD OFF ..... Read Offset
READ CK ..... Read Clock
READ DATA ..... Read Data
RDM INC ..... Read Memory Increment
RCK ..... Read Clock
SCK ..... Servo Clock
SCK1 ..... Servo Clock One
SEEK STROBE ..... Seek Strobe
SL1 ..... Start Load One
SL2 ..... Start Load Two
START ..... Start
SQC ..... Sync QC
SYNC ..... Sync
WRITE DATA ..... Write Data
WØ2·VMA ..... Write Phase Two·Valid Memory Address
μP POWER ..... Microprocessor Power
Ø2 ..... Phase Two
Ø2·VMA ..... Phase Two·Valid Memory Address

## LEGEND FOR 592 BOARD SCHEMATIC

A ..... Disk Address A
ADD0-ADD8 ..... Address Disk
B ..... Disk Address B
C LOAD ..... Control Load
DC LOAD ..... Disk Control Load
DD0-DD7 ..... Disk Data
D HADDL ..... Disk Head Address Load
D INDEX ..... Disk Index
DI STATUS ..... Disk Input Status
DK SEL ..... Disk Select
DRD CLK ..... Disk Read Clock
DRD DATA ..... Disk Read Data
D READ EN ..... Disk Read Enable
D SCK ..... Disk Servo Clock
D WRITE CLK ..... Disk Write Clock
D WRITE DATA ..... Disk Write Data
D WRITE EN ..... Disk Write Enable
FHDADD0-FHDADD8 .. Fixed Head Address
HADDL ..... Head Address Load
HDADD1 ... Head Selection Address Line
HDADD2 ... Head Selection Address Line
HDADD4 ... Head Selection Address Line
HDADD8 ... Head Selection Address Line
ILLEGAL ADD ..... Illegal Address
INDEX A ..... Index A
I STATUS ..... Input Status
MAINT ..... Maintenance
MHDCURSENSE ..... Moving Head Current Sense
MHD MULTSEL ..... Multiple Moving Head Selected
M MODE ..... Maintenance Mode
MOV HDS ..... Moving Heads
OFF FWR ..... Offset Forward
OFF REV ..... Offset Reverse
PWR OK ..... Power OK

Any $\overline{\text{Bar}}$ above any alphabetical or numerical combination indicates line active in a low (0) state.

## 592 BOARD (CONTINUED)

**PWR RST** ..... Power Reset
**RDCLK** ..... Read Clock
**RDDATA** ..... Read Data
**READ EN** ..... Read Enable
**READY** ..... Ready
**RESTORE** ..... Restore
**SCK** ..... Servo Clock
**SEEK COMPLETE** ..... Seek Complete
**SEEK LATE** ..... Seek Late
**SEEK STROBE** ..... Seek Strobe
**SEEK STROBE DLY** ... Seek Strobe Delayed
**SEEK STROBE 1** ..... Seek Strobe One
**STR EARLY** ..... Strobe Early
**STR LATE** ..... Strobe Late
**$\mu$P POWER** ..... Microprocessor Power
**WRITE CLK** ..... Write Clock
**WRITE DATA** ..... Write Data
**WRITE EN** ..... Write Enable
**WRT ADD MK** ..... Write Address Mark
**0 HEAD** ..... Zero Head

## LEGEND FOR 594 BOARD SCHEMATIC

**C LOAD** ..... Control Load
**D INDEX** ..... Disk Index
**D HADDL** ..... Disk Head Address Load
**D READ EN** ..... Disk Read Enable
**D WRITE CLK** ..... Disk Write Clock
**D WRITE DATA** ..... Disk Write Data
**D WRITE EN** ..... Disk Write Enable
**DC LOAD** ..... Disk Control Load

## 594 BOARD (CONTINUED)

**DD0-DD7** ..... Disk Data
**DI STATUS** ..... Disk Input Status
**DRD CLK** ..... Disk Read Clock
**DRD DATA** ..... Disk Read Data
**FAULT CLEAR** ..... Fault Clear
**HADDL** ..... Head Address Load
**HD1,HD2,HD4,HD8** ..... Head Selection Address Lines
**I STATUS** ..... Input Status
**PLO CLK** ..... Phase Lock Osc Clock
**READY** ..... Ready
**SEEK COMPLETE** ..... Seek Complete
**STEP DIR** ..... Step Direction
**TRACK 0** ..... Track Zero
**WRITE CLK** ..... Write Clock
**WRITE FAULT** ..... Write Fault

## SCHEMATIC NOTES

—×— Circuitry not used in some versions.
– – – Circuitry used in some versions.
※ Optional part. Value determined by application
⏚ Ground
▽ Common tie point
Chassis
Flame retardant resistor
⊖ See parts list

Item numbers in rectangles appear in the alignment/adjustment instructions.
Supply voltage maintained as shown in input.
Voltages measured with digital meter.
Terminal indentification may not be found on unit.
Resistors are ¼W or less, 5% unless noted.
Value in ( ) used in some versions.

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